Bala Dhinesh

IIT Madras, Chennai, India
baladhinesh@smail.iitm.ac.in (+91)8610904952 Website @BalaDhinesh @bala-dhinesh

Education

Indian Institute of Technology Madras — **Chennai, India**
B.Tech in Electrical Engineering, Minor in Computing; CGPA 8.63/10 — July 2023
Relevant Coursework:
- Computer Architecture (G), Secure Processor Microarchitecture (G), CAD for VLSI (G), Mapping DSP Algorithms to Arch.(G), Digital System Testing (G), GPU Programming (G), Digital IC Design (G), Computer Organisation, Microprocessors.

*G - Graduate Level Courses

Achievements

- University Demo Best Demonstration, Honorable Mention, SIGDA Design Automation Conference 2021.
- Semi-finalist, Terasic InnovateFPGA design contest 2021 sponsored by Intel, Microsoft and Analog Devices.

Technical Professional Experience

Tenstorrent India Pvt. Ltd. | *Engineer* — July 2023 - Present
- Working with the Design Verification team for the next generation RISC-V microprocessor.

Qualcomm India Pvt. Ltd. | *Hardware Engineering Internship* — May 2022 - Aug 2022
- Automated the development of interrupt-related System Verilog modules for the latest processor.
- Eliminates manually writing of **more than 10K** lines of code | Script is robust, scalable and synthesizable to any microprocessor.

Research Projects

Extreme throughput neural network architecture on FPGA | *Bachelor's Thesis* | *IIT Madras* — Nov 2022 - Present
- Incorporated LUT based neural network training method and highly efficient scalable streaming architecture on hardware.
- Acheived estimated throughput of 1.34M on MobileNetV1 architecture (20x over state-of-the-art).

Approximate Computing on Graph Neural Networks (GNNs) | *Georgia Institute of Technology* — Feb 2022 - Dec 2022
- Replaced the traditional FP32 multipliers in the Graph Convolutional layers with various INT8, INT16 approximate multipliers.
- Reduced the power by **40%** and area by **26%** in matrix multiplication | Accuracy closely similar to FP32 (**70x** gain).
- Examined the effects of approximation component errors | Performed design exploration to determine the **Pareto curve** between power and GNN accuracy | Work is accepted as a poster for the Design Automation Conference (DAC) 2023.

Rapid Hardware Prototyping Framework for FPGAs | *IIT Madras* | Details — Jan 2022 - July 2022
- Developed a remote FPGA lab framework that provides a **ready-to-use harness** for testing user designs on Xilinx FPGAs.
- This setup was used for assignments by more than 130 students enrolled in the Computer Organization (EE2003) course.

Virtual FPGA Lab | *Google Summer of Code 2021* | *FOSSi Foundation* | Details — May 2021 - Aug 2021
- Developed an online simulator to **visualize FPGA** and their peripheral outputs in the Makerchip platform, thereby mimicking the physical FPGA lab experience. Automated the entire **Xilinx Vivado flow** to run the design in an actual FPGA.

Relevant Projects

Custom Data Prefetcher Algorithm | Details
- Replaced Next-Line prefetcher in the IPCP prefetcher with Next or Previous Line prefetcher and simulated using **ChampSim**.
- Achieved **0.73%** improvement in **IPC** and up to **5%** decrease in **MPKC** on the SPEC benchmarks.

RISC-V Bit Manipulation Extension Support | Details
- Implemented **RISC-V Bit Manipulation extension** for RV32 and RV64 in Bluespec SystemVerilog.
- Simulated the design using **Verilator** and **cocotb** is used for writing test benches and verification.

Hardware efficient Bitonic Sorting in Verilog | Details
- Implemented a high-performance Bitonic Parallel sorting algorithm with a reconfigurable number of elements and bitwidth.

Hardware Accelerator for Advanced Encryption Standard (AES) Algorithm | Details
- Accelerated Standard and two security-enhanced modified 128bit AES encryption by designing custom **AXI-Lite IPs** in **Vivado**.
- Interfaced the design with **Microblaze** processor and achieved **35x speedup** and **16%** gain in security performance on FPGA.

RISC-V CPU core | Details
- Implemented a **5-stage pipelined** 32-bit RISC-V ISA processor design in Transaction-Level Verilog (**TL-Verilog**).
- Incorporated **Hazard-detection** and **Data forwarding** units | Tested in Makerchip platform.

Skills

Programming Languages: Verilog, SystemVerilog, TL-Verilog, Bluespec, Python, C/C++, JavaScript, Assembly.
Tools and Softwares: Xilinx Vivado, Vitis, PYNQ, ChampSim, Cachegrind, LT-Spice, Arduino, PyTorch, HLS4ML, cocotb.

Activities

- **Teaching Assistant**, Computer Organisation (EE2003) and Applied Programming Lab (EE2703) courses.
- **Open-source contributor**, Redwood EDA - developing TL-Verilog based educational content and courses.
- Conducted several roadshows on "**Open-source Chip Design using RISC-V**" across India under VLSI System Design.
- **Core, Electronics Club**, Center for Innovation (CFI), IIT Madras - spearheading a team of 50+ Electronics enthusiasts.
- Invited Speaker at **VSDOpen'21** conference - Tutorial trainer on "Digital Design on FPGAs using Makerchip".
- Selected among 1000+ applicants on Computer Architecture winter school by the National Supercomputing Mission, India.